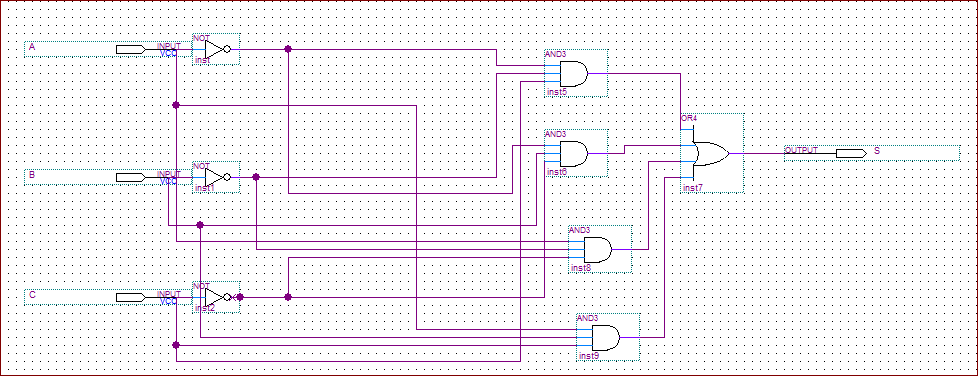
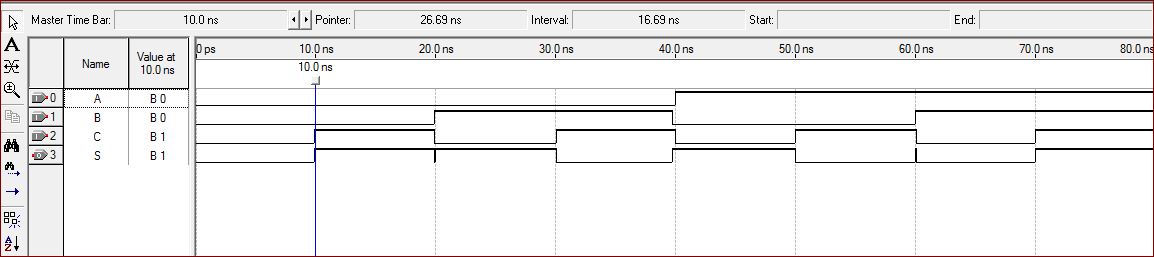
**Answer to the Question No: 01**

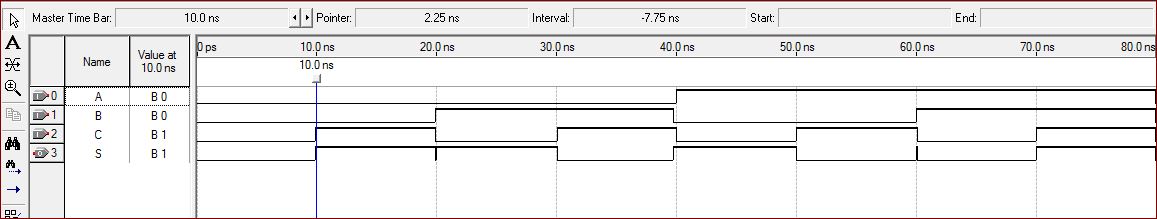


**Figure 1:** Schematic Circuit corresponding to the given function



**Figure 2:** Simulation waveform of the schematic circuit

**Answer to the question no: 02**



**Figure 3:** Simulation waveform of the Verilog code